```
     FILE 'HCAPLUS' ENTERED AT 16:08:49 ON 08 MAR 2002
L1          731 S SILICON ON INSULATOR METAL OXIDE SEMICONDUCTOR OR SOI(W) MOSF
L2           41 S (SILICON(2N)INSULATOR()METAL(2N)MOSFET) OR (SOI(2N)METAL()OXI
L3          715 S SILICON()ON()INSULATOR()METAL()OXIDE()SEMICONDUCTOR OR SOI(W)
L4           17 S (L2 OR L3) NOT L1
L5          106 S L1 AND ((BURY### OR BURIED OR ENCAPSUL? OR CAPSUL? OR ENCAS?)
L6           44 S L5 AND (DRAIN OR DRIFT OR (ACTIVE OR DIFFUSION OR SOURCE)(2N)
L7           29 S L6 AND (GATE OR MEMORY()CELL OR LIBRARY()CELL)
L8           22 S L7 AND (TRENCH## OR HOLE OR GROOVE OR CHANNEL OR EDGE? OR FLU
L9            5 S L8 AND (METAL? OR POLYSILICON)
L10           3 S L4 AND ((BURY### OR BURIED OR ENCAPSUL? OR CAPSUL? OR ENCAS?)
L11           8 S L9 OR L10
L12          17 S L8 NOT L11
```

=> D BIB AB 1-8

```
L11  ANSWER 1 OF 8  HCAPLUS  COPYRIGHT 2002 ACS
AN   2001:617442  HCAPLUS
DN   135:173754
TI   SOI MOSFET devices and fabrication of devices thereof
IN   Fung, Ka Hing
PA   International Business Machines Corp., USA
SO   Jpn. Kokai Tokkyo Koho, 11 pp.
     CODEN: JKXXAF
DT   Patent
LA   Japanese
FAN.CNT 1
     PATENT NO.        KIND  DATE          APPLICATION NO.   DATE
     ---------------   ----  --------      ---------------   --------
PI   JP 2001230423      A2   20010824      JP 2001-78        20010104
     CN 1308378         A    20010815      CN 2000-129498    20001229
PRAI US 2000-481914     A    20000112
AB   The title devices have buried metallic via holes each
     formed directly below body regions each in alignment to gate,
     wherein the buried metal contacts the body region, but does not
     contact source/drain.  The structure provides mutual
     metal connections below the devices where .gtoreq.1 mutual
     connection layers contact the Si insulator film below the devices via a
     buried oxide film.  The arrangement makes possible for
     connection from the bottom of source/drain diffusion layers and
     from the body regions.  The body contacts provides the SOI
     MOSFETs devices with buried metal body contacts for
     compact integration of the circuits.

L11  ANSWER 2 OF 8  HCAPLUS  COPYRIGHT 2002 ACS
AN   2001:401346  HCAPLUS
DN   135:145216
TI   Formation of SiGe on insulator structure and approach to obtain highly
     strained Si layer for MOSFETs
AU   Sugiyama, Naoharu; Mizuno, Tomohisa; Suzuki, Masamichi; Takagi, Sin-Ichi
CS   Advanced LSI Technology Laboratory, Corporate R&D Center, Toshiba
     Corporation, Kawasaki, 212-8582, Japan
SO   Jpn. J. Appl. Phys., Part 1 (2001), 40(4B), 2875-2880
     CODEN: JAPNDE; ISSN: 0021-4922
PB   Japan Society of Applied Physics
DT   Journal
LA   English
AB   The formation of a SiGe layer on insulators, which can be realized by
     applying the sepn. by implanted oxygen (SIMOX) technique to SiGe layers,
     is essential for fabricating strained silicon on insulator (SOI)
     metal oxide semiconductor field effect
     transistors (MOSFETs).  In this study, the SIMOX process for SiGe films is
     examd. in terms of Ge diffusion during SIMOX annealing and the annealing
     temp.  It is found that the SIMOX annealing at temp. above 1300.degree. is
     necessary to realize uniform buried oxides, even
     though the m.p. of SiGe crystal decreases with the Ge content.  Ge
     diffusion during high-temp. annealing must also be taken into account when
     prepg. the SiGe layer for SIMOX.  These facts indicate that the
     realization of a SiGe layer on buried oxides is
     difficult with the simple SIMOX process for SiGe crystal, particularly so
     in the case of high Ge content.  In order to overcome this problem, the
     double layer SiGe structure on an insulator is proposed and the
     effectiveness of this structure on the increase of strain in Si is
```

. verified exptl. The strain relaxation of the SiGe layer with higher Ge content, which is grown on the SiGe layer with lower Ge content, is obsd. with expanding of the under-layer.

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 3 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:113438 HCAPLUS
DN 134:359888
TI Designing nanometer silicon-on-**insulator** MOSFET with **buried** Si1-xGex quantum well **channel**
AU Fu, Y.; Patel, C. J.; Willander, M.
CS Physical Electronics and Photonics, Department of Physics, University of Goteborg and Chalmers University of Technology, Goteborg, S-412 96, Swed.
SO Physica E (Amsterdam, Neth.) (2001), 9(4), 694-700
CODEN: PELNFM; ISSN: 1386-9477
PB Elsevier Science B.V.
DT Journal
LA English
AB The authors study the device characterization of Si-on-insulator (SOI) **metal**-oxide-semiconductor field effect transistor (MOSFET) with buried Si1-xGex quantum well (QW) **channel**. Accurate quantum mech. description of the p-**channel** of the buried Si1-xGex QW shows that the peak carrier concn. in the conduction **channel** is higher in the pos. graded SiGe QW, whereas the carriers are more uniformly distributed in the retrograded QW. By phenomenol. introducing a phys. parameter to describe the energy relaxation of transmitting wave due to various scattering processes, systematic simulation about quantum wave transmissions of the authors' **SOI MOSFET** indicates normal current-bias characteristics at nanometer regime. A threshold **gate** bias of .apprx.0.6 V was obtained for both the pos. graded and retrograded Si-Ge QWs.

RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 4 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:96502 HCAPLUS
DN 128:211476
TI Effects of **buried oxide** stress on thin-film **silicon**-on-**insulator metal-oxide-semiconductor** field-effect transistor
AU Lee, Jong-Wook; Nam, Myung-Hee; Oh, Jeong-Hee; Yang, Ji-Woon; Lee, Won-Chang; Kim, Hyung-Ki; Oh, Min-Rok; Koh, Yo-Hwan
CS Semiconductor Research Division, Hyundai Electronics Industries Co., Ltd., Ichon-si, Kyoungki-do, 467-860, S. Korea
SO Appl. Phys. Lett. (1998), 72(6), 677-679
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB Thin-film Si-on-insulator (SOI) device characteristics were studied in terms of stress in the **buried oxide** interface by both simulation and expt. Bonded SOI wafer with a 400 nm **buried oxide** and SOI wafer with a 100 nm **buried oxide** which is made by implanted O were used as a substrate for device fabrication. From the simulation, the 100 nm **buried oxide** has higher compressive stress than the 400 nm counterpart after the local oxidn. of Si process. With the highly compressive-stressed **buried oxide**, B atoms may

accumulate at the Si side, esp. at the Si **edge**, under tensile stress so that these accumulated B atoms increase threshold voltage of the **edge channel**. Therefore, there is no hump of the **drain** current in the subthreshold **drain** current-**gate**-voltage characteristics of thin-film SOI n-**channel** **metal**-oxide-semiconductor field-effect transistors (MOSFET) with the highly compressed **buried oxide**.

L11 ANSWER 5 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:722923 HCAPLUS
DN 128:55872
TI An analytical symmetric double-**gate silicon**-on-**insulator metal-oxide-semiconductor** field-effect-transistor model
AU Jang, Sheng-Lyang; Hu, Man-Chun; Liu, Shau-Shen
CS National Taiwan University of Science and Technology, Taipei, 106, Taiwan
SO Jpn. J. Appl. Phys., Part 1 (1997), 36(10), 6250-6253
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB A new complete and anal. **drain** current model for sym. double-**gate** Si-on-insulator **metal**-oxide-semiconductor field-effect-transistors (**SOI MOSFETs**) is presented. The model applicable for digital/analog circuit simulation contains the following advanced features: precise description of the subthreshold, near threshold and above-threshold regions of operation by one single expression and consideration of the source/**drain** resistance. It includes important short **channel** effects such as velocity satn., **drain** induced barrier lowering and **channel** length modulation, self-heating effect due to the low thermal cond. of the **buried oxide**, and impact-ionization of MOS devices and parasitic bipolar junction transistor assocd. with **drain** breakdown. It was developed using a quasi-two-dimensional Poisson equation.

L11 ANSWER 6 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:354400 HCAPLUS
DN 127:102494
TI An analytical fully depleted **silicon**-on-**insulator metal-oxide-semiconductor** field-effect-transistor model considering the effects of self-heating, source/**drain** resistance, impact-ionization, and parasitic bipolar junction transistor
AU Hu, Man-Chun; Jang, Sheng-Lyang; Chen, Young-Shying; Liu, Shau-Shen; Lin, Jien-Min
CS Department Electronic Engineering, National Taiwan Institute Technology, Taipei, 106, Taiwan
SO Jpn. J. Appl. Phys., Part 1 (1997), 36(5A), 2606-2613
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB This paper presents a simple, complete, and anal. **drain** current model for a submicrometer silicon-on-insulator MOSFET transistor (**SOI MOSFET**). The model applicable for digital/analog circuit simulation contains the following advanced features: precise description of the subthreshold, near threshold, and above-threshold regions of operation by one single expression; precise description of I-V

.and G-V characteristics in the satn. region; single-piece **drain** current equation smoothly continuous from the linear region to satn. **region**; considering the **source/drain** resistance; inclusion of important short **channel** effects such as velocity satn., **drain** induced barrier lowering, and **channel** length modulation; self-heating effect due to the low thermal cond. of the **buried oxide**; impact ionization of MOS devices and the parasitic bipolar junction transistor (BJT) effect assocd. with **drain** breakdown. The model predicts that the parasitic resistances are important for submicron and deep submicron SOI MOS devices, the effects of impact-ionization and parasitic BJT was important in satn. region at small **gate** source voltage VGF, and the self-heating effect is important in the satn. region at large VGF. The present model agrees well with exptl. results of various dimensions.

L11 ANSWER 7 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:321189 HCAPLUS
DN 122:175609
TI Analysis of SIMOX metal-oxide-semiconductor transistors operated in the high temperature range
AU Ouisse, T.; Reichert, G.; Cristoloveanu, S.; Faynot, O.; Giffard, B.
CS Laboratoire de Physique des Composants a Semiconducteurs (URA-CNRS 840), ENSERG, BP257, 38016, Grenoble, Fr.
SO Mater. Sci. Eng., B (1995), B29(1-3), 21-3
CODEN: MSBTEK; ISSN: 0921-5107
DT Journal
LA English
AB A systematic study of the phys. properties and performance of SIMOX Si-on-insulator (**SOI**) **metal-oxide-semiconductor** field effect transistors, operated from 210 to 625 K is presented. SOI devices are attractive candidates for minimizing leakage currents at high temp. The surface mobility follows conventional behavior. The sensitivity of the SIMOX **buried oxide** to hot carrier injection is found to exhibit a max. at an intermediate temp., around 400 K.

L11 ANSWER 8 OF 8 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:205872 HCAPLUS
DN 120:205872
TI Device simulation of a thin-film silicon on insulator power metal-oxide-semiconductor field-effect transistor for structure optimization
AU Matsumoto, Satoshi; Yoshino, Hideo
CS Interdiscripl. Res. Lab., NTT, Musashino, 180, Japan
SO Jpn. J. Appl. Phys., Part 1 (1994), 33(1B), 519-23
CODEN: JAPNDE; ISSN: 0021-4922
DT Journal
LA English
AB This paper proposes an optimized device structure based on the results of numerically simulating thin-film Si on insulator (**SOI**) power **metal-oxide-semiconductor** field-effect transistors (MOSFETs) in the 50-V class. The dependence of the breakdown voltage and specific on-resistance on the doping concn. of the drain offset region, on the thickness of the superficial Si layer, on the thickness of the **buried oxide** layer, and on the drain offset length are compared for buried channel MOSFETs and surface channel MOSFETs.

=> D BIB AB 1-17

L12 ANSWER 1 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:109743 HCAPLUS
TI Clarification of floating-body effects on drive current and short **channel** effect in deep sub-0.25 .mu.m partially depleted **SOI MOSFETs**
AU Matsumoto, Takuji; Maeda, Shigenobu; Hirano, Yuuichi; Eikyu, Katsumi; Yamaguchi, Yasuo; Maegawa, Shigeto; Inuishi, Masahide; Nishimura, Tadashi
CS ULSI Development Center, Mitsubishi Electric Corporation, Hyogo, 664-8641, Japan
SO IEEE Transactions on Electron Devices (2002), 49(1), 55-60
CODEN: IETDAI; ISSN: 0018-9383
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB We point out for the first time that floating-body effects cause the redn. of the satn. drive current in partially depleted (PD) **SOI MOSFETs**. It is demonstrated that when the **channel** concn. of the **SOI MOSFETs** is set higher in order to suppress the increase of the off current caused by floating-body effects, the drive current decreases due to the large body effect. In the conventional SOI structure where the source-**drain** junction is in contact with the **buried oxide**, the 0.18 .mu.m floating PD **SOI MOSFET** suffers around 17% decrease in the drive current under the same threshold voltage (Vth) in comparison with body-fixed one. However, floating PD **SOI MOSFETs** show smaller Vth-roll-off. Further considering the short **channel** effect down to the min. **gate** length of 0.16 .mu.m, the current decrease becomes 6%. Also, we propose a floating PD **SOI MOSFET** with shallow source-**drain** junction (SSD) structure to suppress the floating-body effects. By using the SSD structure, we confirmed an increase in the drive current.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 2 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:72773 HCAPLUS
DN 136:127697
TI Method for making **SOI MOSFET**
IN Oh, Jeong Hee
PA Hynix Semiconductor Inc., S. Korea
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002009859	A1	20020124	US 2001-891193	20010626
	JP 2002033490	A2	20020131	JP 2001-170062	20010605
PRAI	KR 2000-37414	A	20000630		

AB Disclosed is a method for making an **SOI MOSFET**, which is capable of improving threshold voltage variations and a parasitic bipolar effect generated in the formation of fully depleted (FD) SOI semiconductor integrated circuits using a recess **channel**. The method involves the steps of forming a **buried oxide** film and an active silicon film over a silicon-on-insulator substrate,

forming a **channel** at a recess **channel**, forming dummy spacers at opposite side walls of the etched active silicon film, forming a **gate** between the dummy spacers, forming a photoresist film on the **gate** and the active silicon film, forming lightly doped **drain** regions, removing the dummy spacers, forming lightly doped ion regions, resp., forming spacers at opposite side walls of the recess **channel** region, resp., removing the photoresist film, forming a **source region** and a **drain region**, forming **source/drain** electrodes and a **gate** electrode on the resultant structure.

L12 ANSWER 3 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:763499 HCAPLUS
DN 135:297131
TI SOI semiconductor integrated circuit for eliminating floating body effects in **SOI MOSFETs** and method of fabricating the same
IN Kim, Young-wug; Kim, Byung-sun; Kang, Hee-sung; Ko, Young-gun; Park, Sung-dae; Kim, Min-su; Kim, Kwang-il
PA Samsung Electronics,co. Ltd, S. Korea
SO U.S. Pat. Appl. Publ., 33 pp., Cont.-in-part of U.S. Ser. No. 695,341.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001031518	A1	20011018	US 2001-782116	20010213
PRAI	US 1999-161479	P	19991025		
	US 2000-695341	A2	20001024		

AB A Si-on-insulator (SOI) integrated circuit and a method of fabricating the SOI integrated circuit are provided. At least 1 isolated transistor **active region** and a body line are formed on an SOI substrate. The transistor **active region** and the body line are surrounded by an isolation layer which is in contact with a **buried insulating** layer of the SOI substrate. A portion of the sidewall of the transistor **active region** is extended to the body line. Thus, the transistor **active region** is elec. connected to the body line through a body extension. The body extension is covered with a body insulating layer. An insulated **gate** pattern is formed over the transistor **active region**, and 1 end of the **gate** pattern is overlapped with the body insulating layer.

L12 ANSWER 4 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:747271 HCAPLUS
DN 135:281691
TI Design and fabrication of a **SOI MOSFET** semiconductor device
IN Adan, Alberto O.
PA Sharp Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 21 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1143527	A1	20011010	EP 2001-302968	20010329

R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,

IE, SI, LT, LV, FI, RO
JP 2001284591 A2 20011012 JP 2000-102359 20000404
US 2001028089 A1 20011011 US 2001-822251 20010402
CN 1316781 A 20011010 CN 2001-117888 20010404
PRAI JP 2000-102359 A 20000404
AB A semiconductor device of SOI structure comprises a surface semiconductor layer in a floating state, which is stacked on a **buried insulating** film so as to construct an SOI substrate, **source/drain regions** of 2nd cond. type which are formed in the surface semiconductor layer, a **channel** region of 1st cond. type between the **source/drain regions** and a **gate** electrode formed on the **channel** region through a **gate** insulating film; in which the surface semiconductor layer has a potential well of the 1st cond. type formed therein at and/or near at least one end of the **channel** region in a **gate** width direction thereof.
RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 5 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:237407 HCAPLUS
DN 134:359953
TI "Gated-diode" configuration in **SOI MOSFET**'s: a sensitive tool for evaluating the quality and reliability of the buried Si/SiO2 interface
AU Zhao, Xuejun; Salman, Akram; Ioannou, Dimitris E.; Jenkins, William C.; Hughes, Harold L.
CS ECE Department, George Mason University, Fairfax, VA, 22030, USA
SO AIP Conf. Proc. (2001), 550(Characterization and Metrology for ULSI Technology), 226-230
CODEN: APCPCS; ISSN: 0094-243X
PB American Institute of Physics
DT Journal
LA English
AB A gated-diode configuration in **SOI MOSFET**'s is described, which is particularly suitable and easy to use for characterizing the **buried oxide** interface. This new approach becomes possible by taking advantage of the front **gate**, which is biased to inversion (NMOSFET's) or accumulation (BC-PMOSFET's) during the measurement. As a result, the **drain** merges with the inversion or accumulation layer and extends under the entire **gate**, forming a horizontal p-n junction with the **channel**. The **drain**-to-body diode is then forward-biased by a small voltage, and the back **gate** voltage is scanned such that it brings the back interface to depletion, a condition that is at the center of all gated-diode techniques and required to activate the interface states and start the recombination/generation processes. The midchannel interface state d. was obtained from the peak of the measured current vs. back **gate** voltage curves, and by combining the measurements with 2-dimensional numerical simulations (e.g. a combination of SUPREM and PISCES), the interface state d. profiles along the **channel** length near the source and **drain** can also be obtained.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 6 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:31776 HCAPLUS
DN 134:109030
TI Lateral thin-film silicon-on-insulator (SOI) device having a **gate**

03/08/2002

electrode and a field plate electrode
IN Simpson, Mark; Letavic, Theodore
PA Koninklijke Philips Electronics N.V., Neth.
SO PCT Int. Appl., 15 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 5

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001003201	A1	20010111	WO 2000-EP5956	20000627
	W: CN, JP, KR				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 6346451	B1	20020212	US 1999-343912	19990630
	EP 1118125	A1	20010725	EP 2000-943905	20000627
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
PRAI	US 1999-343912	A	19990630		
	US 1997-998048	A2	19971224		
	WO 2000-EP5956	W	20000627		

AB A lateral thin-film Si-On-Insulator (SOI) device includes a semiconductor substrate, a **buried insulating** layer on the substrate and a lateral transistor device in an SOI layer on the **buried insulating** layer and having a **source region** of a 1st cond. type formed in a body region of a 2nd cond. type opposite to that of the 1st. A lateral **drift** region of a 1st cond. type is provided adjacent the body region, and a **drain** region of the 1st cond. type is provided laterally spaced apart from the body region by the **drift** region. A **gate** electrode is provided over a part of the body region in which a **channel** region is formed during operation and extending over a part of the lateral **drift** region adjacent the body region, with the **gate** electrode being at least substantially insulated from the body region and **drift** region by an insulation region. In order to provide improved breakdown voltage characteristics, a dielec. layer is provided over at least a part of the insulation region and the **gate** electrode, and a field plate electrode is provided over at least a part of the dielec. layer which is in direct contact with the insulation region, with the field plate electrode being connected to an electrode of the lateral transistor device.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 7 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:479683 HCAPLUS
DN 133:66530
TI An analytical model for fully depleted single **gate** SOI MOS transistors including lattice temperature effects
AU Gharabagi, Roobik
CS Department of Electrical Engineering, St Louis University, St Louis, MO, 63156, USA
SO Int. J. Electron. (2000), 87(2), 129-136
CODEN: IJELA2; ISSN: 0020-7217
PB Taylor & Francis Ltd.
DT Journal
LA English
AB An anal. model for fully depleted **SOI MOSFETs** is presented. Major small geometry effects such as carrier velocity satn.,

mobility degrdn., **channel** length modulation, and **drain** induced barrier lowering are included. Device self-heating due to low thermal cond. of a **buried oxide** layer is included in carrier mobility modeling. Thermal effects are also included in threshold voltage expression. Source, **drain**, and **channel** resistance effects are also included. Modeled results are compared to available measured data and are shown to be in very good agreement.

RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 8 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:212716 HCAPLUS
DN 132:230290
TI The behavior of narrow-width **SOI MOSFET**'s with MESA isolation
AU Wang, Hongmei; Chan, Mansun; Wang, Yangyuan; Ko, Ping K.
CS Peking University, Beijing, Peop. Rep. China
SO IEEE Trans. Electron Devices (2000), 47(3), 593-600
CODEN: IETDAI; ISSN: 0018-9383
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Narrow-width effects in thin-film silicon-on-insulator (**SOI**) **MOSFET**'s with MESA isolation technol. have been studied theor. and exptl. As the **channel** width of the MOSFET is scaled down, the **gate** control of the **channel** potential is enhanced. It leads to the suppression of **drain** current dependence on substrate bias and punch-through effect in narrow-width devices. The variation of threshold voltage with the **channel** width is also studied and is found to have a strong dependence on thickness of silicon film, interface charges in the **buried oxide**, and **channel** type of **SOI MOSFET**.

RE.CNT 20 THERE ARE 20 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 9 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:362975 HCAPLUS
DN 131:123623
TI An analytical symmetric double-**gate SOI MOSFET** model
AU Jiou, Hong-Kee; Jang, Sheng-Lyang; Liu, Shau-Shen
CS Kuang Wu Institute of Technology and Commerce, Taipei, Taiwan
SO Int. J. Electron. (1999), 86(6), 671-683
CODEN: IJELA2; ISSN: 0020-7217
PB Taylor & Francis Ltd.
DT Journal
LA English
AB In this paper, we present a simple, complete and anal. **drain** current model for sym. double-**gate SOI MOSFETs**. The model was developed using a quasi-two-dimensional Poisson's equation. The model, applicable to digital/analog circuit simulation, contains the following advanced features: precise description of the sub-threshold, near threshold and above-threshold regions of operation by one single expression; single-piece **drain** current equation, smoothly continuous from the linear region to the satn. **region**, considering the **source/drain** resistance; inclusion of important short **channel** effects such as velocity satn., **drain**-induced barrier lowering and **channel** length modulation; self-heating effect due to the low thermal cond. of the

buried oxide; impact-ionization of MOS devices; and the parasitic BJT effect assocd. with **drain** breakdown.

RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 10 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:196456 HCAPLUS
DN 130:203867
TI **SOI-MOSFET** and fabrication process thereof
IN Adan, Alberto O.
PA Sharp Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 17 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 902482	A1	19990317	EP 1998-305138	19980629
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 11087719	A2	19990330	JP 1997-241482	19970905
	US 6288425	B1	20010911	US 1998-99107	19980618
PRAI	JP 1997-241482	A	19970905		

AB A **SOI-MOSFET** includes: a substrate; a **buried oxide** film formed on the substrate; a top semiconductor layer formed on the **buried oxide** film, said top semiconductor layer having a portion of a 1st cond. type; a **gate** electrode formed on the top semiconductor layer with a **gate** oxide film interposed there between; **source** and **drain regions** of a 2nd cond. type formed in the top semiconductor layer and on both sides of the **gate** electrode;. And an embedded region of the 2nd cond. type which is disposed in the top semiconductor layer and between the **source** and **drain regions** and is sepd. from the **source** and **drain regions** and from an interface between the top semiconductor layer and the **gate** oxide film. The embedded region is defined by a tilted implantation of ions of the 1st cond. type, using the **gate** electrode as a mask. The **SOI-MOSFET** has a fully depleted surface **channel** due to the contact potential between said surface **channel** and the embedded region, whereby the Kink effect is prevented.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 11 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:353036 HCAPLUS
DN 129:11616
TI Semiconductor device and its fabrication
IN Maeda, Shigenobu; Yamaguchi, Yasuo; Iwamatsu, Toshiaki
PA Mitsubishi Denki K. K., Japan; Maeda, Shigenobu; Yamaguchi, Yasuo; Iwamatsu, Toshiaki
SO PCT Int. Appl., 76 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI WO 9822983 A1 19980528 WO 1996-JP3369 19961115
W: JP, KR, US
RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE
EP 948057 A1 19991006 EP 1996-938489 19961115
R: DE, FR, GB
US 2001045601 A1 20011129 US 1998-169903 19981009
PRAI WO 1996-JP3369 W 19961115
AB An SOI layer is formed on a Si substrate with a **buried insulating** layer in between. In the SOI layer , **SOI-MOSFET** having a **drain area** and a **source area** which are so formed to define a **channel**-forming area and a **gate** electrode layer facing the **channel** forming area with an insulating layer in between is formed. There is provided a field-shield (FS) isolation structure in which an FS plate which faces to the area of the SOI layer near the ends of the **drain** and **source areas** through the insulating layer is provided and the **SOI-MOSFET** is elec. isolated from other elements by fixing the potential at the area of the SOI layer facing the plate by imparting a predetd. potential to the FS plate. The **channel** forming area has 2 end sections in the **channel** width direction and a central part between both end sections, and the **channel** length of the area in the end sections of the area is shorter than that in the central part.

L12 ANSWER 12 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:280563 HCAPLUS
DN 129:74580
TI Short **channel** effects in sub-0.1 .mu.m thin film **SOI-MOSFETs**
AU Rauly, E.; Balestra, F.
CS Laboratoire de Physique des Composants a Semiconducteurs (UMR CNRS/INPG). ENSERG, Grenoble, 38016, Fr.
SO Electron. Lett. (1998), 34(7), 700-701
CODEN: ELLEAK; ISSN: 0013-5194
PB Institution of Electrical Engineers
DT Journal
LA English
AB Short **channel** effects are thoroughly investigated in sub-0.1 .mu.m N **channel SOI-MOSFETs** by using a two-dimensional numerical simulation. **Drain**-induced barrier lowering and charge sharing effects are calcd. as a function of the main device parameters for **gate** lengths down to 0.05 .mu.m. The impact of the silicon layer, the **gate oxide** and the **buried oxide** thicknesses, as well as of the Si film doping, are shown.

L12 ANSWER 13 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:62273 HCAPLUS
DN 128:122610
TI High-voltage lateral **SOI MOSFET** having a semiconductor linkup region
IN Merchant, Steven L.
PA Philips Electronics North America Corp., USA
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1
PATENT NO. KIND DATE APPLICATION NO. DATE

```
     ---------------  ----  --------       ---------------  --------
PI   US 5710451       A     19980120       US 1996-629819   19960410
     WO 9738447       A2    19971016       WO 1997-IB246    19970313
     WO 9738447       A3    19980129
         W:  JP, KR
         RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE
     EP 843899        A2    19980527       EP 1997-905348   19970313
         R:  DE, FR, GB, IT, NL
     JP 11508091      T2    19990713       JP 1997-535994   19970313
PRAI US 1996-629819         19960410
     WO 1997-IB246          19970313
```

AB A semiconductor-on-insulator (SOI) device includes a semiconductor substrate, a **buried insulating** layer on the substrate, and a lateral MOSFET on the **buried insulating** layer. The MOSFET includes a semiconductor surface layer on the **buried insulating** layer and has a **source region** of a 1st cond. type, a **channel** region of a 2nd cond. type, an insulated **gate** electrode over the **channel** region, a lateral **drift** region of the 2nd cond. type, and a **drain** region of the 1st cond. type laterally spaced from the **channel** region by the **drift** region. A semiconductor linkup region of the 1st cond. type is provided between the **channel** region and the **drift** region and extending substantially through the semiconductor surface layer, and the **source region** of the device is elec. coupled to the **drift** region. This device configuration is particularly useful in providing a high-voltage p-**channel** MOS transistor using thin SOI high-voltage technol. normally assocd. with fabricating n-**channel** devices.

L12 ANSWER 14 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:497374 HCAPLUS
TI The role of the **buried oxide** in the hot-carrier degradation of ultra thin n-**channel SOI-MOSFETs**
AU Huttner, T.; Mahnkopf, R.; Wurzer, H.; Bielb, M.; Abstreiter, G.
CS Semiconductor Div., Dept. HL PI M, Siemens AG, Munchgen, D-81730, Germany
SO Proc. - Electrochem. Soc. (1997), 97-23(Silicon-on-Insulator Technology and Devices), 277-282
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB The influence of front **channel** hot-carrier stress on the **buried oxide** of ultra thin (45 nm) n-**channel SOI-MOSFETs** with 0.28 .mu.m effective **channel** length on SIMOX substrates has been studied. A method is proposed to det. sep. damage at the front **gate oxide** and **buried oxide**. **Hole** capturing and interface state generation as well have been identified as damaging mechanisms. The generated **buried oxide** interface states are located at the **drain** side of the transistor. Although the **buried oxide** was heavily damaged, the front **channel** is only slightly affected. Nevertheless, the **buried oxide** damage can not be neglected, as its influence increases with stress time.

L12 ANSWER 15 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:497338 HCAPLUS
DN 127:227903
TI Short **channel** effects in sub-0.1 .mu.m **SOI-**

MOSFETs
AU Rauly, E.; Balestra, F.
CS lab. Phys. Composants Semiconducteurs (UMR-CNRS), ENSERG-INPG, Grenoble, 38016, Fr.
SO Proc. - Electrochem. Soc. (1997), 97-23(Silicon-on-Insulator Technology and Devices), 227-232
CODEN: PESODO; ISSN: 0161-6374
PB Electrochemical Society
DT Journal
LA English
AB Short **channel** effects (SCE) were investigated in sub-0.1 .mu.m N **channel SOI-MOSFETs** with two-dimensional numerical simulation. The **Drain**-Induced Barrier Lowering (DIBL) and the charge sharing (CS) effects are calcd. as a function of the main device parameters for **gate** lengths down to 0.05 .mu.m. The thinning of the silicon layer and the **gate** oxide leads to a substantial decrease of SCE, whereas the **buried oxide** has only a slight influence. The impact of the doping of the silicon film is also pointed out.

L12 ANSWER 16 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:393594 HCAPLUS
DN 127:102580
TI 0.18-.mu.m Fully-depleted silicon-on-insulator MOSFET's
AU Cao, Min; Kamins, Ted; Voorde, Paul Vande; Diaz, Carlos; Greene, Wayne
CS ULSI Research Laboratory, Hewlett-Packard Laboratories, Palo Alto, CA, 94304, USA
SO IEEE Electron Device Lett. (1997), 18(6), 251-253
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB High-performance 0.18-.mu.m **gate**-length fully-depleted silicon-on-insulator (FD-**SOI**) **MOSFET**'s were fabricated using 4-nm **gate** oxide, 35-nm thick **channel**, and 80-nm or 150-nm **buried oxide** layer. An elevated source/ **drain** structure was used to provide extra silicon during silicide formation, resulting in low source/**drain** series resistance. Nominal device drive currents of 560 .mu.A/.mu.m and 340 .mu.A/.mu.m were achieved for n-**channel** and p-**channel** devices, resp., at a supply voltage of 1.8 V. Improved short-**channel** performance and reduced self-heating were obsd. for devices with thinner **buried oxide** layers.

L12 ANSWER 17 OF 17 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:92035 HCAPLUS
DN 120:92035
TI Simulation and two-dimensional analytical modeling of subthreshold slope in ultrathin-film **SOI MOSFET**'s down to 0.1 .mu.m **gate** length
AU Joachim, Hans Oliver; Yamaguchi, Yasuo; Ishikawa, Kiyoshi; Inoue, Yasuo; Nishimura, Tadashi
CS LSI Lab., Mitsubishi Electr. Corp., Itami, 664, Japan
SO IEEE Trans. Electron Devices (1993), 40(10), 1812-7
CODEN: IETDAI; ISSN: 0018-9383
DT Journal
LA English
AB The subthreshold slope in ultrathin-film fully depleted **SOI MOSFET**'s is investigated for **channel** lengths from the

long **channel** region down to 0.1 .mu.m. A doping effect is found which allows the authors to improve the S-factor by increasing the **channel** doping concn. In order to explain this phenomenon and to clarify the mechanism of S-factor degrdn. at short **gate** length, a two-dimensional anal. model is developed. A modified boundary condition is introduced for the two-dimensional Poisson equation to account for the nonlinear potential distribution inside the **buried oxide**
. The S-factor short **channel** degrdn. is governed by three mechanisms: the rise of capacitances at the **channel** source and **drain** ends due to the two-dimensional potential distribution; the subthreshold current flow at the back **channel** surface; and the modulation of the effective current **channel** thickness during the **gate** voltage swing in the subthreshold region. The anal. model results are compared to those of numerical device simulation, and a good agreement is found. The model can be utilized to predict design criteria for miniaturized thin-film fully depleted **SOI MOSFET**